
Article:
Kawai, H., Yagi, S., Hirata, S. et al. (7 more authors) (2017) Low cost high voltage GaN polarization superjunction field effect transistors. Physica Status Solidi (a). ISSN 1862-6300

https://doi.org/10.1002/pssa.201600834

Low cost high voltage GaN polarization superjunction field effect transistors

Hiroji Kawai [*,1], S Yagi[1], S. Hirata[1], F. Nakamura[1], T. Saito[1], Y. Kamiyama[1], M. Yamamoto[2], H. Amano[3], Vineet Unni[4] and E.M.S. Narayanan[4]

[1] Powdec KK, 1-23-15 Wakagi-cho, Oyama city, Tochigi 323-0028, Japan
[2] Shimane University, Matsue-shi, Shimane 690-8504, Japan
[3] Nagoya University, Furo-cho, Chikusa-ku, Nagoya, 464-8601, Japan
[4] University of Sheffield, Velocity 2, 3 Solly Street, Sheffield S1 4DE, United Kingdom

Received ZZZ, revised ZZZ, accepted ZZZ
Published online ZZZ (Dates will be provided by the publisher.)

Keywords 2DHG, superjunction, gallium nitride, low-cost production

* Corresponding author: e-mail kawai@powdec.co.jp, Phone: +81-285-22-9986, Fax: :+81-285-22-9987

A comprehensive overview of novel high voltage GaN field effect transistors (FETs) based on the Polarization Superjunction (PSJ) concept and a cost-effective approach towards manufacturing these high performance devices are presented. Current challenges impeding wider adoption of GaN power switching transistors in applications, and latest results of scaled-up PSJ-FETs from POWDEC KK, have also been discussed. The article also presents hard-switching characteristics of 400V-to-800V boost converter constructed using a PSJ-FET grown on sapphire substrate and the future direction of GaN power semiconductor technology based on monolithic integration for advanced power electronics.

1 Introduction It has been more than two decades since the demonstration of the world's first Gallium Nitride (GaN) p-n homojunction LEDs and the world's first high electron mobility transistors (HEMTs) based on a GaN-$Al_xGa_{1-x}N$ heterojunction [1, 2]. Although lighting and radio-frequency application segments have achieved remarkable commercial success using GaN, the technology readiness of high voltage power switching transistors is still in a nascent stage. The development roadmap of GaN power semiconductor devices is currently geared towards power conversion systems in existing applications such as Power Factor Correction (PFC), AC/DC to DC converters, power-conditioning circuits as well as emerging applications in aerospace (More Electric Aircraft) and automotive sectors (Electric/Hybrid Electric Vehicles), with voltage rating between 600 V and 1.2 kV. Most of the commercial players (e.g., GaN Systems, Infineon, ON Semiconductor, Panasonic, and Transphorm) have focussed on 600V GaN devices, and off-the-shelf samples are now available from some of these. However, it needs to be recognized that despite the decade-long concerted efforts by the power semiconductor industry and academia likewise, manufacturing of GaN power switching transistors can still be considered to be in the pre-production stage in general, with little to no penetration in the market. This article will briefly discuss the challenges concerning present mainstream GaN field effect transistors (FETs) and present GaN polarization superjunction field effect transistors (PSJ-FETs) as an alternative solution. An overview of the PSJ technology, the latest performance results of high voltage GaN PSJ-FETs and a detailed assessment of the cost-effective production using this technology platform will be presented.

2 Current challenges Figure 1 shows the cross-sectional schematic of a conventional GaN HFET on Silicon (Si) substrate, and the distribution of the electric field under off-state conditions. The limitation in performance of such devices is attributable to the following main reasons:

(a) As the distribution of the electric field under off-state conditions is not uniform, realizing high voltage devices requires sophisticated processing capability for for-

mation of field modulating plates, which can significantly increase processing time and costs.

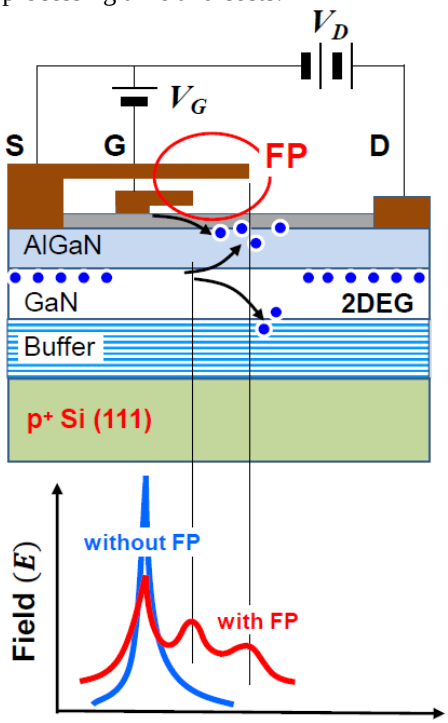


Figure 1 Simplified schematic of conventional HFET cross-section and electric field distribution under off-state conditions.

(b) Localised peaking of the electric field during off-state condition renders such devices sensitive to current collapse during high voltage switching [3].

(c) The growth of GaN epitaxial layers on Si substrates for high voltage applications requires thick buffer and transition layers which make the wafers more susceptible to bowing and crack generation [4, 5].

(d) The inherent tensile stress due to mismatch in lattice constants and coefficients of thermal expansion in such structures can also compromise the reliability of devices.

(e) Due to the vertical nature of breakdown in GaN-on-Si FETs, breakdown voltage of the device is primarily determined by the GaN buffer thickness [6, 7].

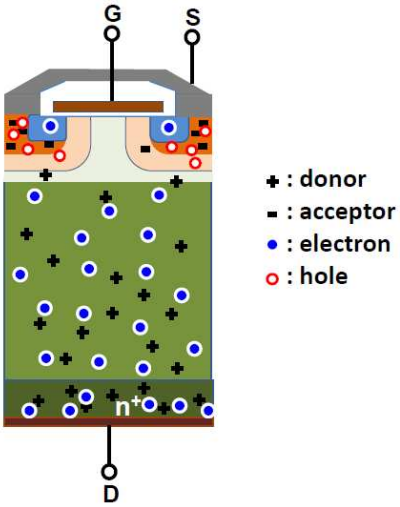
(f) Lack of avalanche capability or non-destructive breakdown behaviour, necessitates the need for over-rating the device breakdown voltage for a given application.

(g) The most recent results on crosstalk have indicated that the Si substrate has to be maintained at ground potential to mitigate the crosstalk effects in monolithic GaN-on-Si devices [8, 9]. But it has also been reported that performance of GaN-on-Si devices with grounded substrate terminal, deteriorated (increased on-state resistance (R_{ON})) when employed as a high-side switch in a half-bridge circuit [10]. These two challenges can hamper the development of monolithic integration in GaN-on-Si platform.

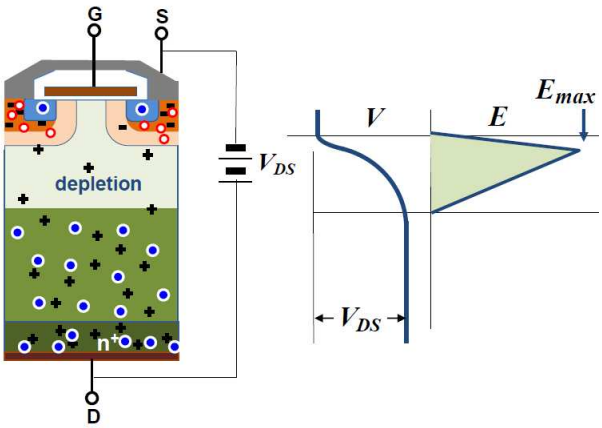
An alternative solution for manufacturing low-cost high-voltage GaN power switching devices, which can overcome almost all of the above-mentioned challenges, is the adoption of Polarization Superjunction (PSJ) implemented on sapphire substrate, as described in the next section.

3 Polarization Superjunction

3.1 Superjunction Simplified schematics of the cross-section of a conventional power MOSFET and the electric field profile in the device under off-state conditions have been shown in Figures 2 (a)-(b) respectively.



(a)



(b)

Figure 2 Schematic of (a) cross-section of a conventional power MOSFET (b) electric field distribution under off-state conditions.

Under off-state condition and application of a drain bias voltage, the depletion region in the n- epi layer in a con-

ventional power MOSFET primarily extends in the vertical direction. When electric field at the p n- junction reaches the critical electric field of Si, the device undergoes avalanche breakdown. Breakdown voltage (BV) is essentially determined by the thickness and doping concentration of the n- epi layer. Therefore, BV for a given drift thickness can only be enhanced by reducing the doping concentration in the n- region which results in a significant increase (proportional to BV^2) in the specific on-state resistance ($R_{ON}.A$).

The concept of superjunction (SJ) transformed the capability of Si power MOSFETs by taking the device performance beyond the one-dimensional theoretical limit using an innovative approach to achieving charge balance in the structure.

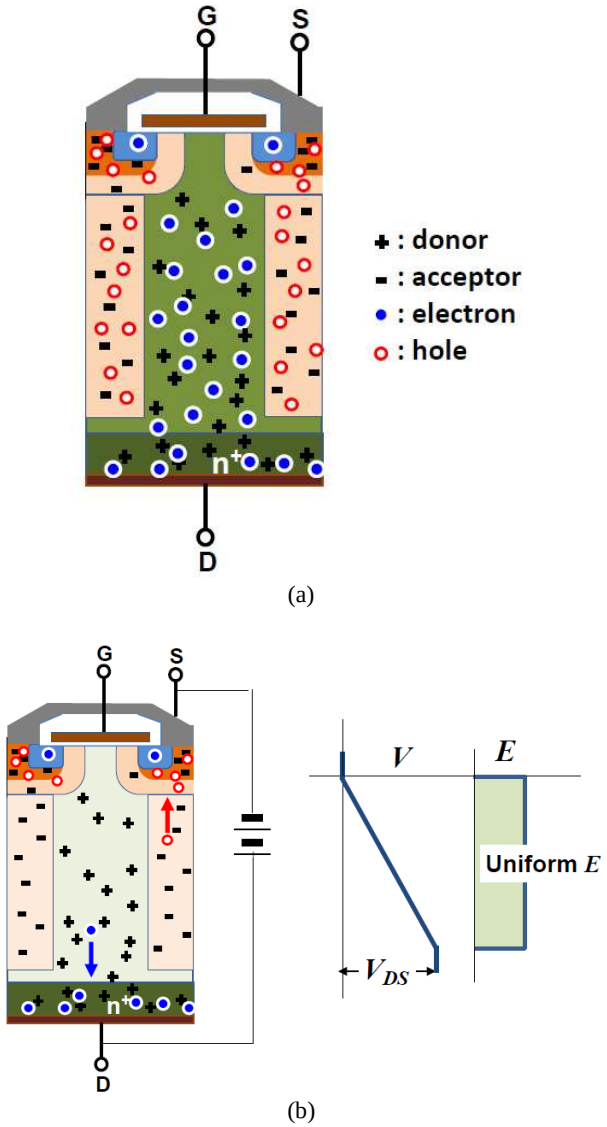


Figure 3 Schematic of (a) cross-section of a superjunction power MOSFET (b) electric field distribution under off-state conditions.

As shown in Figure 3, SJ devices incorporate a number of alternately stacked p- and n-type heavily and precisely doped layers. Under off-state conditions, and high drain bias, the depletion region in such a device extends laterally as well as vertically in the entire drift region, as observed in conventional RESURF structures [11-14]. The improved field shaping that is achieved translates to higher BV for a given drift thickness, significantly enhancing the device figure of merit.

Theoretically, a flat field distribution of the electric field can be achieved in a SJ power MOSFET compared to a triangular field profile that is obtained in a conventional power MOSFET.

3.2 Polarization Superjunction Realizing SJ devices mandates precise control of p- and n-type doping in the semiconductor. However, doping control has been problematic in GaN, especially with achieving p-type doping due to high activation energy of Mg that is typically used as the dopant [15]. Polarization Superjunction (PSJ) is a unique technique to achieve charge balance not through impurity-based doping control, but by engineering of positive and negative polarization charges inherent in the GaN material. PSJ technology is based on a GaN/AlGaN/GaN double heterostructure (grown along the (0001) crystal axis) where positive and negative polarization charges coexist at the AlGaN $(000\bar{1})$/GaN(0001) interface with two-dimensional electron gas (2DEG) accumulation and GaN$(000\bar{1})$/AlGaN(0001) interface with two-dimensional hole gas (2DHG) accumulation respectively [16-23]. The basic concept/structure has been illustrated in Figure 4.

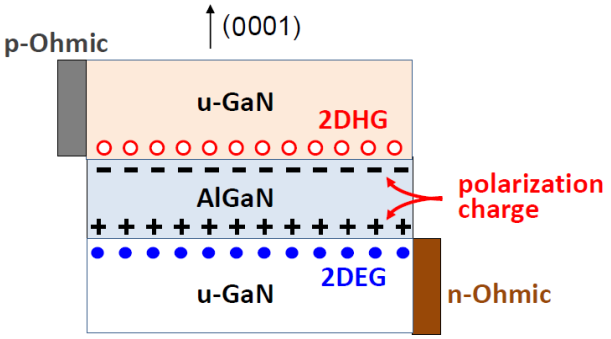
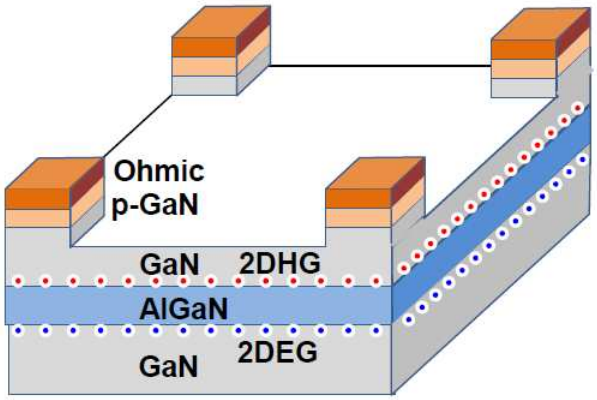


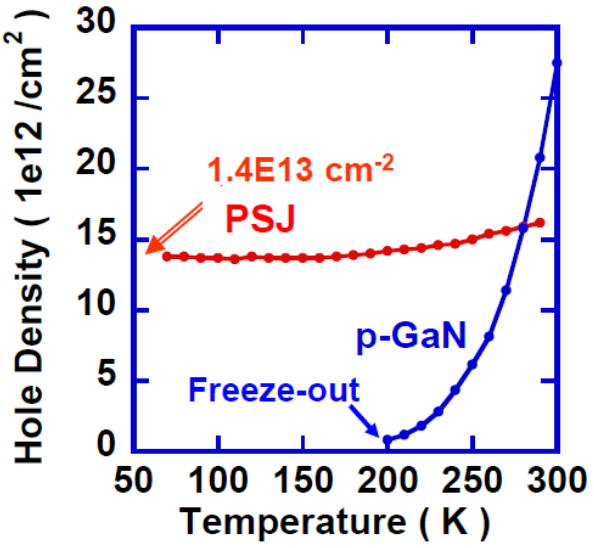
Figure 4 Schematic illustration of a PSJ structure.

2DEG and 2DHG are well-confined to quantum wells at the respective interfaces and possess enhanced mobility because of negligible impurity scattering. Despite theoretical predictions of high density 2DHG induced by negative polarization charges at such interfaces (GaN$(000\bar{1})$/AlGaN(0001)), the first demonstration of high density 2DHG of over $1x10^{13}$ cm^{-2} was achieved by researchers at the University of Sheffield, United Kingdom and POWDEC K.K, Japan in 2010 [17]. Schematic of the four-point probe measurement of hole characteristics with-

in the optimised structure using van der Pauw method, has been shown in Figure 5 (a). By optimizing the layer thicknesses and the growth conditions of the GaN/AlGaN/GaN double heterostructure, 2DHG as high as $1.4x10^{13}$ cm^{-2} has been obtained as determined from Hall Effect measurements and shown in Figure 5 (b).



(a)

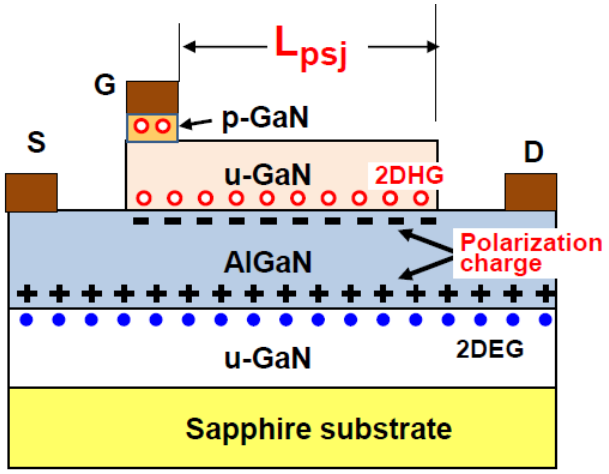


(b)

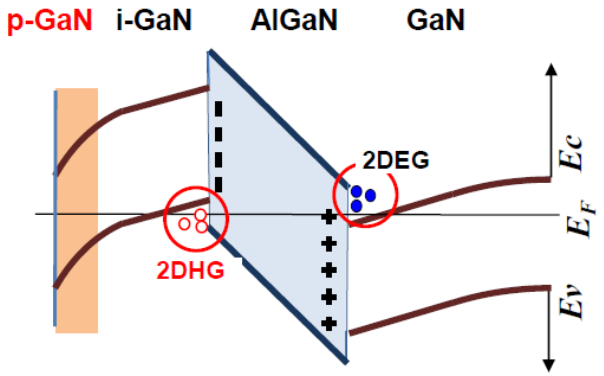
Figure 5 (a) Schematic of van der Pauw test structure for measuring hole characteristics (b) measured two-dimensional hole gas density and hole density arising due to impurity doping, as a function of temperature.

As can be noted, the 2DHG density in the PSJ structure does not change significantly with temperature (50 K – 300 K), unlike Mg doping in a reference specimen with single p-GaN layer, where carriers freeze-out at low temperatures (~ 200 K)). This indicates that the holes truly originate due to polarization effects in the PSJ structure.

3.3 Polarization Superjunction Field Effect Transistors (PSJ-FET) Figures 6 (a)-(b) show simplified cross section of a normally-on PSJ-FET as well as the energy band diagram in the double heterostructure under thermal equilibrium. Also shown in the band diagram is the accumulation of 2DEG and 2DHG at the two heterojunctions. In this device architecture, gate makes an ohmic contact to the p-GaN layer and 2DHG. Drain and source electrodes form ohmic contacts to 2DEG. In the on-state, current flows from the drain to source electrode through the 2DEG in a manner similar to the conventional AlGaN/GaN HFETs.



(a)



(b)

Figure 6 (a) Schematic of a PSJ FET (b) energy band diagram at thermal equilibrium.

The drift region that maintains charge balance in the device is positioned between the gate and drain electrodes. Figures 7 show the simplified cross-section of this device under off-state conditions and in the presence of a drain bias. 2DHG and 2DEG are discharged through the gate and drain electrodes, respectively, and the drift region is depleted at low drain bias voltage. The electric field profile

during blocking state and under ideal charge balance conditions in the drift region has also been depicted in Figure 7. Due to the "box like" electric field shape, the blocking voltage capability of PSJ devices can be scaled-up directly as a function of the length of the PSJ region (L_{PSJ}).

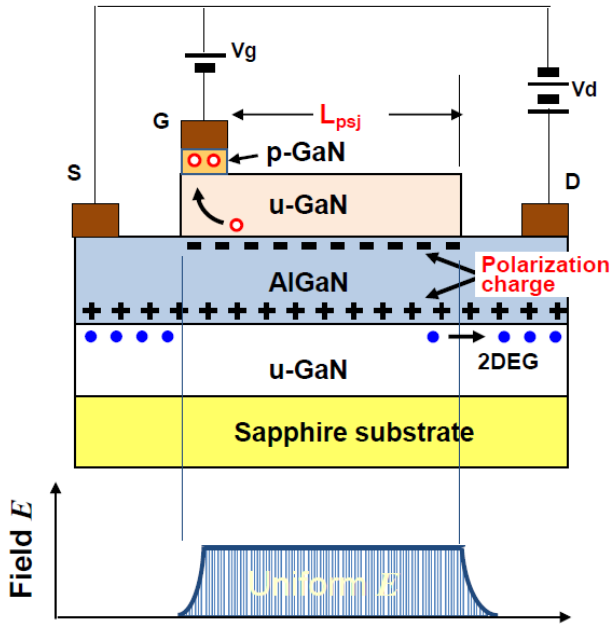


Figure 7 Schematic of a PSJ FET under blocking state and the electric field profile under ideal charge balance conditions.

3.4 Performance Figure 8 shows photographs of a fabricated large area PSJ-FET die (size: 6 mm x 4 mm) fabricated on sapphire substrate as well as a packaged device (TO-247) from POWDEC KK.

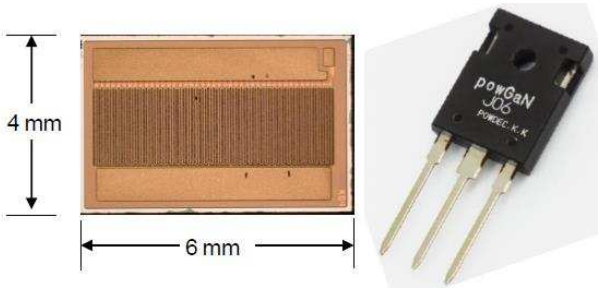
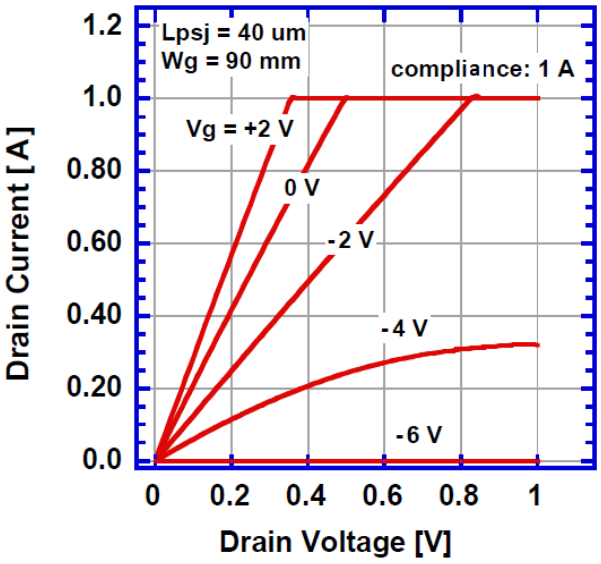
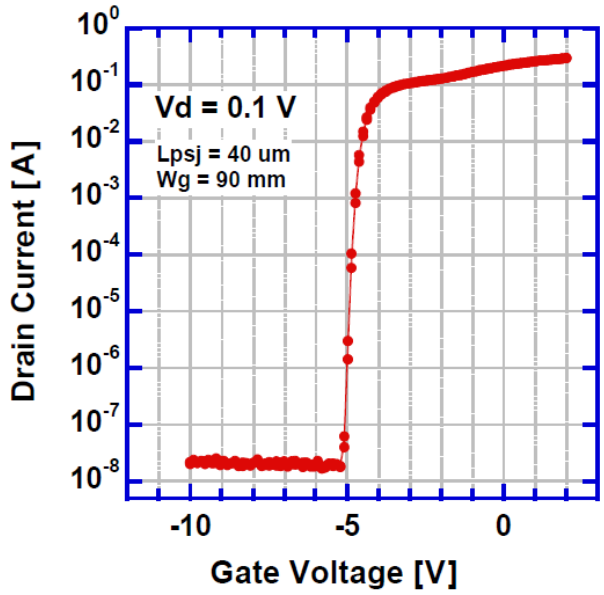


Figure 8 Photograph of a PSJ FET die and a packaged unit.

Output I-V characteristics of a typical device (gate width Wg = 90 mm, L_{PSJ} = 40 µm) have been shown in Figure 8 (a). The compliance current during measurement was set as 1A. The on-state resistance was measured as 350 mΩ at a gate voltage (Vg) = +2V. Transfer characteristics (drain voltage (Vd) = 0.1 V) have been shown in Figure 8 (b). The typical threshold voltage (V_{TH}) is about -4.5 V, with excellent sub-threshold characteristics. The minimum value of the sub-threshold slope has been observed to be about 70 mV/decade, which is quite close to the theoretically predicted value of about 59 mV/decade. The remarkable sub-threshold characteristics can be attributed primarily to the reason that these PSJ-FETs have been fabricated on sapphire which is an excellent insulating substrate.



(a)

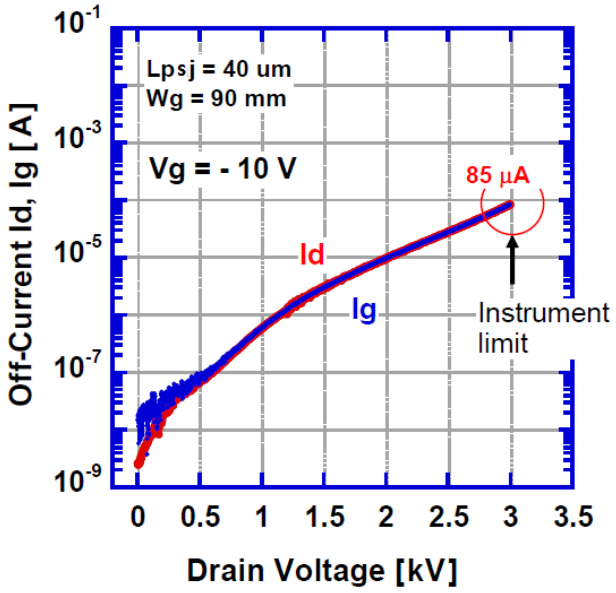


(b)

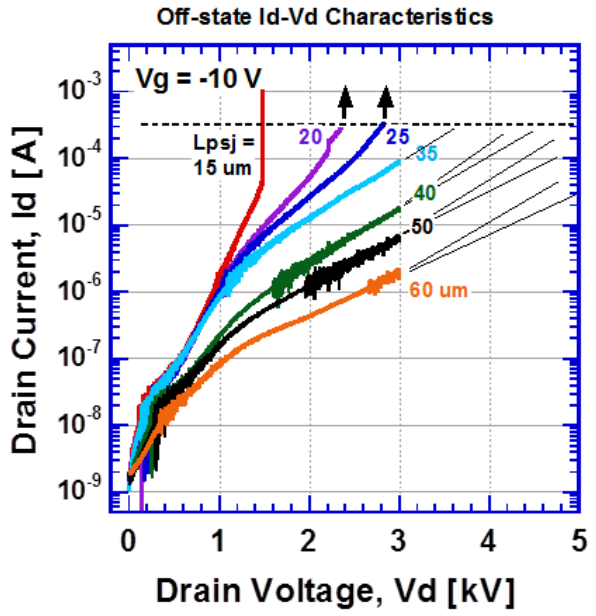
Figure 8 Measured (a) output I-V characteristics (b) DC transfer characteristics

Off-state drain and gate current as a function of drain voltage have been shown in Figure 9 (a). The actual BV of the measured PSJ-FET (L_{PSJ} = 40 µm) is greater

than 3 kV. The leakage current was measured to be ~ 85 µA at 3 kV, and it was observed that Id and Ig were identical. This confirmed that the leakage path was directed from drain to gate in PSJ-FETs on sapphire substrates.



(a)



(b)

Figure 9 Measured off-state characteristics at Vgs = - 10V of fabricated (a) PSJ-FET (L_{PSJ}=40µm, Wg= 90 mm) (b) PSJ-FETs with various PSJ lengths (L_{PSJ}). The noises seen in the current range between 10^{-8} and 10^{-6} ampere are due to the sensitivity of the B1505A analyser.

Figure 9 (b) depicts the plot of the leakage current characteristics for a series of samples, with various L_{PSJ} (from 15 µm to 60 µm), as a function of drain voltage. Based on careful extrapolation, BV of PSJ devices on sapphire with L_{PSJ}= 60 µm, is expected to be in the range of 6 to 7 kV. A linear relation can be observed between BV and L_{PSJ}, which is a fundamental characteristic of superjunction devices.

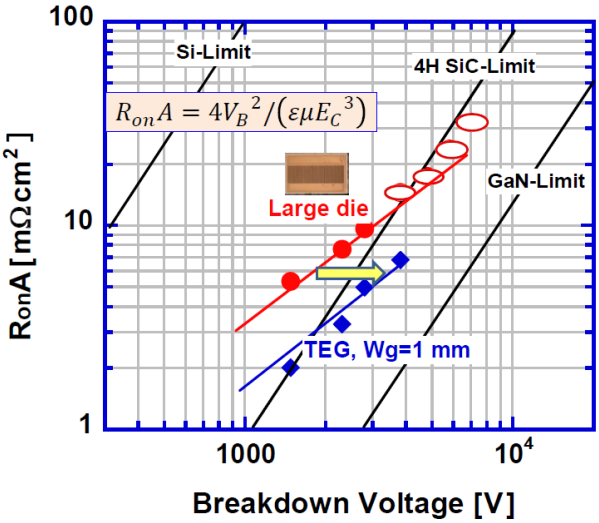


Figure 10 Specific on-state resistance (R_{ON}.A) versus breakdown voltage of fabricated PSJ-FETs on sapphire (large area and device test structures). The empty ellipses are the extrapolated values from Fig.9(b) and RonA (not shown here).

Based on the measured on-state and off-state electrical characteristics, the relationship between area-specific on-state resistance (R_{ON}.A) and BV of fabricated PSJ-FETs on sapphire substrates has been plotted in Figure 10. Also shown in the figure are the theoretical one-dimensional material limits for Si, 4H-Silicon Carbide (4H-SiC) and GaN. It is well established that in conventional devices R_{ON}.A increases proportionally to the second order of BV, whereas in superjunction devices, R_{ON}.A is directly proportional to BV [24]. Such a linear relation has been confirmed for PSJ-FETs. It can be deduced from the figure that BV in such devices can be enhanced with moderate increase of R_{ON}.A by merely increasing the gate-to-drain distance (L_{PSJ}). It was also observed from the plots that the device test structures (labelled as TEG) show R_{ON}.A values which are almost half of the values obtained for large area devices with the same L_{PSJ} and blocking capability. This trend clearly indicates that there is room for further improvement in the performance of the scaled-up large area devices.

Dynamic characterisation was also performed on the large area PSJ-FETs primarily to examine the current collapse behaviour (also described as increase in the on-state resistance during high voltage switching) in these devices

[3]. The schematic of the measurement circuit and the waveforms obtained have been shown in Figure 11. The applied voltage was approximately 1 kV, and the load resistance chosen was 200 Ω to fix the device on-state current at 5 A. High voltage stress was applied for 10 seconds, at the end of which, a gate pulse was applied for a duration of 1 µs. As shown in Figure 11, with an applied gate bias (3V), the on-state current of the PSJ-FET rises to 5A and Vd drops sharply with a fall time (t_f) of 50 ns. Therefore, no dynamic current collapse was observed in PSJ-FETs in this experiment.

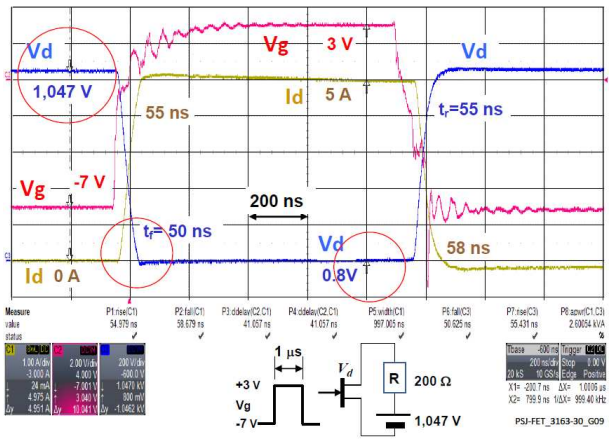


Figure 11 PSJ-FET switching characteristics.

It needs to be emphasized that PSJ-FETs do not employ any field modulating plates within the structure, typically used in conventional HFETs for breakdown enhancement and minimizing current collapse [3]. Tanaka et al. have recently suggested that hole injection during off-state can suppress current collapse in GaN Gate Injection Transistors [25]. The superior current collapse performance of PSJ-FETs, can be fundamentally attributed to the enhanced field shaping achieved intrinsically within the double heterostructure.

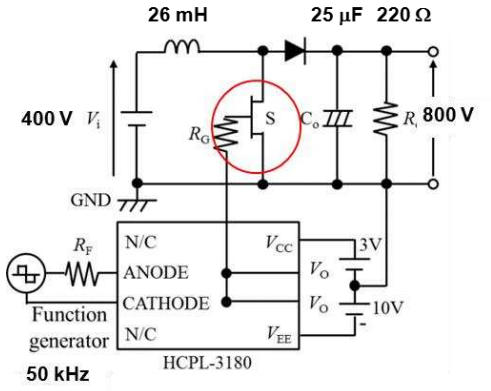


Figure 12 Circuit diagram of the 400 V-800 V boost converter.

In order to demonstrate the advantage of PSJ-FETs in power converter applications, a 400V-800V boost converter was constructed. Typical applications of such converters include regulated dc power supplies, LED drivers, and regenerative breaking of dc motors [26]. The schematic of the configured circuit has been shown in Figure 12.

A signal with +3 V high and -10 V low was applied to the gate of the PSJ-HFET using a HCPL-3180 driver driven with a 50% duty cycle pulse train from a function generator. The pulse period was set as 20 µs (50 kHz). Hard-switching characteristics and waveforms have been shown in Figure 13.

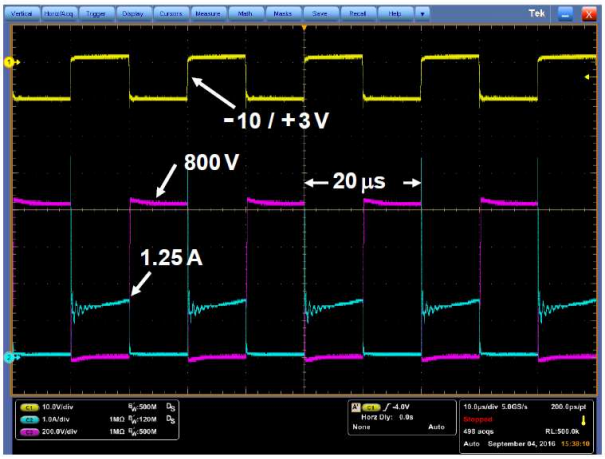


Figure 13 Hard-switching characteristics of the 400V-800V boost converter using PSJ-FETs. The red line shows the drain current and the blue line shows the inductor current.

The L_{PSJ} and on-state resistance (R_{ON}) of the device used in this experiment was 20 µm and 130 mΩ, respectively. Therefore, by strengthening the power source ~~circuit parameters~~ and thermal management, the output power of the converter could be scaled up to a few kW~~9kW~~. To the authors' knowledge, this is the first report of an 800V circuit implementation using an ~~all GaN~~ normally-on power switching transistor.

Thermal management is a critical component of power system design that affects the functionality, power density, robustness, as well as efficiency of power electronic devices and circuits. In order to verify the heat dissipation capability of PSJ-FET fabricated on sapphire substrates, time response of current conduction in a packaged GaN PSJ-FET and a commercial SiC-MOSFET in the absence of air-blowing/cooling was examined. Both devices used for comparison in this study were packaged in TO-247 and had the same on-state resistance of 160 mΩ. The results of the evaluation have been shown in Figure 14 and indicate that the PSJ-FET could maintain a current higher than that of the SiC device, under the same conditions. The

results suggest that the effective thermal resistance of the PSJ-FET appears to be smaller than its SiC counterpart, despite being fabricated on a sapphire substrate. These results seem counter-intuitive considering that sapphire has a lower thermal conductivity than SiC. The thermal resistance of a sapphire substrate (4 mm x 6mm, 100 µm thick) was therefore investigated ~~and found~~ to be ~ 0.1^0C/W. ~~quite competitive when compared to typical package thermal resistance. Another~~ Temperature dependence of Ron increase between the two is found to be almost the same, Therefore, a possible reason for the improved thermal characteristics of PSJ-FET could be due to the lower current density per area and hence the lower temperature because of its die size when compared to the vertical SiC die, which is ~20% smaller.

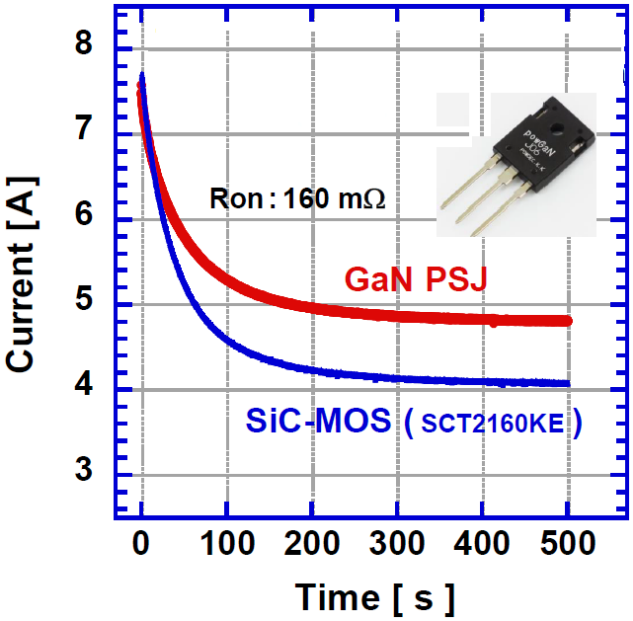


Figure 14 Time response of current conduction in a GaN PSJ-FET and a SiC-MOSFET in the absence of air-blowing/cooling.

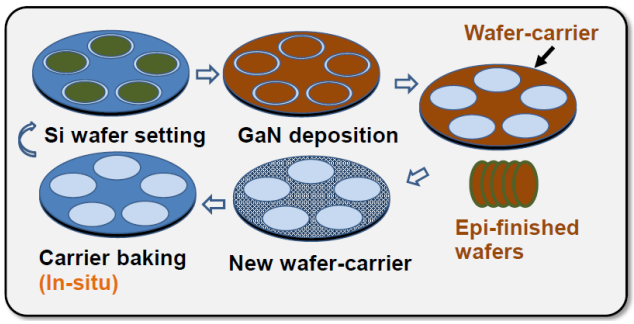
One of the key advantages of using sapphire as the starting substrate is also its suitability for developing monolithic power integrated circuits. This has been discussed further in the last section of this article.

3.5 Low-cost manufacturing Despite having a multitude of remarkable characteristics and enormous efforts from academia and industry, GaN power semiconductor devices have experienced a relatively slow progress towards commercialisation. Beyond some of the scientific and technological challenges, the key reason behind this scenario is the high cost of manufacturing these devices. The growth of GaN epitaxial layers on Si substrates is more difficult than on sapphire substrates. There are two main reasons behind this.

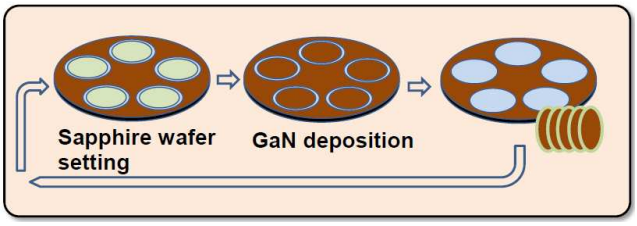
i. Gallium (Ga) reacts with Si easily and degrades the Si surface. Therefore, a thick Aluminium Nitride (AlN) barrier layer must be deposited during the initial phase of the growth. The AlN growth rate must be kept low to prevent a gas-phase reaction with ammonia.

ii. Poor crystal quality of the GaN grown on Si substrate. Growth of a high quality buffer layer is required in order to obtain a reasonable crystal quality, and the growth of this layer takes a very long time (total growth time is approximately half a day).

On the other hand, the growth on sapphire is relatively less complex, and is an established process due to the availability of existing infrastructure and processing capability for GaN LED production. Another important advantage of GaN-on-sapphire is that the breakdown is determined by the lateral shaping of the electric field. This is unlike GaN-on-Si, where there is a vertical component which determines the breakdown voltage of the device mandating thicker epi layers for higher blocking capability. In GaN PSJ-FETs, the epi-thickness required is only 1 µm. The low epi-thickness that is independent of the blocking voltage requirement enables reduced cycle time for growth. As mentioned earlier in this section, the reaction of Ga with Si during GaN epitaxial growth degrades the Si substrate. Due to this, the wafer carrier has to be replaced by a new one and baked in-situ, after each growth run. On the other hand, the growth on sapphire can run consecutively numerous times without interruption. This key aspect has been illustrated in Figures 15 (a) - (b).



(a)



(b)

Figure 15 GaN growth sequence in production (a) GaN-on-Silicon (b) GaN-on-Sapphire.

The overall cost of manufacturing GaN-on-Si epi-wafers encompasses expenses related to the Si substrate, reactor cleaning, and the deposition cost for thick epi layers. Apart from the benefits of an uninterrupted growth cycle, it needs to be considered that the price of a 6-inch sapphire substrate is today approximately only twice that of a silicon (111) substrate. Due to the mentioned reasons, in the manufacturing of GaN-on-Si, added indirect costs and increased production time make it economically/technologically less competitive on the whole when compared to GaN-on-sapphire.

3.6 Future There are several scientific, technological and manufacturing challenges that need to be addressed before GaN power semiconductor devices can be considered mainstream. It is also becoming apparent that a transition from the general scheme of manufacturing power conversion circuits using discrete devices to that of a fully integrated power system-on-chip, rather than being an aspect of evolution in technology development, is anticipated to be a prerequisite to fully harness the high-frequency power switching benefits of GaN [23, 27]. GaN transistors can switch at very high speeds with voltage slew rates of 100 - 300 V/ns and current slew rates in the tens of A/ns. Such high slew rates in the presence of device/package/circuit parasitic inductance can cause substantial over-voltage transients on device terminals, which can degrade/damage the device during operation. Although this is traditionally addressed using damping techniques such as external gate resistors to reduce the overshoot, it results in lower efficiency [28]. Parasitic inductance of the gate drive loop is typically minimized through chip-scale packaging (CSP) by keeping lead lengths and traces as short as possible on the printed circuit board [29]. Even with the most innovative packaging/hybrid-integration solutions, finite residual inductance leads to high frequency oscillations that can not only inadvertently modify the transistor switching state, cause electromagnetic interference, but also damage the device.

By monolithically integrating gate drive circuitry with power devices on a single technology platform, the energy efficiency can be greatly enhanced. Monolithic integration is also considered an ideal approach to minimize parasitic inductance in the circuitry and therefore enable stable high-frequency operation, efficiency and power densities unachievable by existing techniques based on co-packaging discrete devices. A simplified block diagram illustrating a monolithic integration scheme in GaN has been shown in Figure 16. Monolithic integration in GaN has gained some attention over the last few years, but has been mostly restricted to low voltage operation [30-33]. Development of CMOS logic and drive circuits is also essential and towards that end, there have been efforts on demonstration of GaN-based enhancement-mode p-channel and n-channel HFETs [34, 35]. Such an integrated approach can enable higher power switching frequency in circuits yielding significant reduction of filter sizes. Moreover, reduction in the overall bill of materials and wide range of temperature-operation using all-GaN solutions can offer system level performance/cost benefits in existing and emerging applications such as Internet of Things, communications, photonics, radar, aerospace, automotive & data centres.

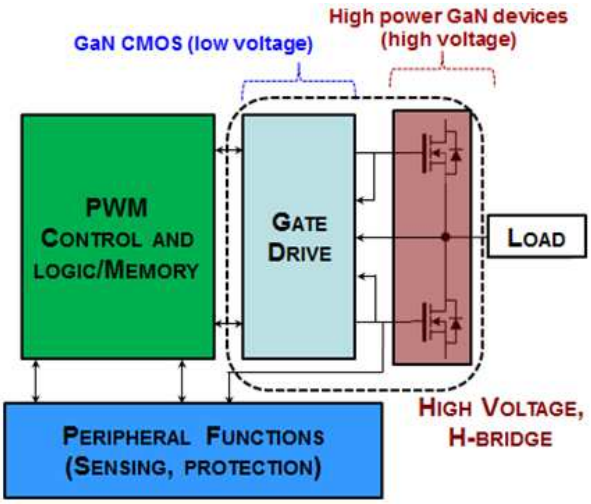


Figure 16 Simplified block diagram illustrating monolithic integration (represented by dashed lines) in a GaN Power Management Integrated Circuit (PMIC) [23].

The fundamental requirement of a semiconductor technology platform that enables simultaneous development of a wide range of high voltage and low voltage devices in GaN as required for integration is served by the PSJ platform [16-23]. Unlike GaN-on-Si, GaN-on-sapphire doesn't suffer from crosstalk issues, due to the excellent insulating properties of sapphire. Along with the recent results on the investigation of sapphire's thermal characteristics as described in this article indicate that GaN PSJ-on-sapphire will prove to be a promising technology platform for next-generation ultra-high power density systems-on-chip.

3.7 Concluding remarks In this article, an overview of novel high voltage polarization superjunction technology platform in GaN materials system is presented. With extremely competitive performance trade-offs, PSJ devices are ideally suited for extreme operating conditions and can be used in space, aerospace, transportation, oil-drilling, industrial as well as consumer applications. A sustainable route towards manufacturing of PSJ-FETs, utilizing the existing and mature infrastructure for GaN LED production, has also been discussed in this article. This will overcome the key hurdle of cost that is generally associated with any

wide bandgap semiconductor slowing down its acceptance as a mainstream power semiconductor technology. With sapphire as the chosen substrate, PSJ is also ideally suited for developing monolithic power integrated circuits which will be essential for practically realising high frequency power switching solutions using GaN. In conclusion, GaN PSJ technology will be instrumental in shaping a viable and a new era of advanced power electronics.

Acknowledgements Vineet Unni acknowledges the support of EPSRC Doctoral Prize Fellowship provided by EPSRC and the University of Sheffield for contributing to this work.

References

[1] H. Amano, M. Kito, K. Hiramatsu, and I. Akasaki, Jpn. J. Appl. Phys. **28**, L2112 (1989).
[2] M. Asif Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson, Appl. Phys. Lett., **63**, 1214 (1993).
[3] W. Saito, Y. Kakiuchi, T. Nitta, Y. Saito, T. Noda, H. Fujimoto, A. Yoshioka, T. Ohno, and M. Yamaguchi, IEEE Electron Device Lett., **31**, 659 (2010).
[4] A. Krost and A. Dadgar, Phys. Status Solidi A **194**, 361 (2002).
[5] D. Zhu, D. J. Wallis, and C. J. Humphreys, Rep. Prog. Phys. **76**, 106501 (2013).
[6] D. Visalli, M. V. Hove, P. Srivastava, J. Derluyn, J. Das, M. Leys, S. Degroote, K. Cheng, M. Germain, and G. Borghs, Appl. Phys. Lett. **97**, 113501-1 (2010).
[7] M. Bin Lu, E. L. Piner, and T. Palacios, Proc. Device Res. Conf., Notre Dame, USA, 2010, pp. 193–194.
[8] V. Unni, H. Kawai, and E. M. S. Narayanan, Microelectronics Reliability **54**, 2242 (2014).
[9] Q. Jiang, Z. Tang, C. Zhou, S. Yang, and K. J. Chen, IEEE Trans. Electron Devices **61**, 3808 (2014).
[10] V. Unni, H. Kawai, and E. M. S. Narayanan, Electronics Lett. **51**, 108 (2014).
[11] J. A. Appels and H. M. J. Vaes, Proc. Int. Electron Devices Meeting, 1979, pp. 238-241.
[12] D. J. Coe, US Patent # 4754310 (1988).
[13] T. Fujihira, Jpn. J. Appl. Phys. **36**, 6254 (1997).
[14] G. Deboy, M. Marz, J. P. Stengel, H. Strack, J. Tihanyi, and H. Weber, Proc. Int. Electron Devices Meeting, 1998, pp. 683-685.
[15] U. Kaufmann, P. Schlotter, H. Obloh, K. Kohler, and M. Maier, Phys. Rev. B, **62**, 10867 (2000).
[16] A. Nakajima, K. Adachi, M. Shimizu, and H. Okumura, Appl. Phys. Lett. **89**, 193501-1 (2006).
[17] A. Nakajima, Y. Sumida, M. H. Dhyani, H. Kawai, and E. M. S. Narayanan, Appl. Phys. Express. **3**, 121004-1 (2010).
[18] A. Nakajima, Y. Sumida, M. H. Dhyani, H. Kawai, and E. M. S. Narayanan, IEEE Electron Device Lett. **32**, 542 (2011).
[19] A. Nakajima, M. H. Dhyani, Y. Sumida, H. Kawai, and E. M. S. Narayanan, Proc. Int. Symp. Power Semiconductor Devices and ICs, 2011, pp. 280-283.
[20] A. Nakajima, V. Unni, K. G. Menon, M. H. Dhyani, Y. Sumida, H. Kawai, and E. M. S. Narayanan, Proc. Int. Symp. Power Semiconductor Devices and ICs, 2012, pp. 265-268.
[21] V. Unni, H. Long, M. Sweet, A. Balachandran, A. Nakajima, H. Kawai, and E. M. S. Narayanan, Proc. Int. Symp. Power Semiconductor Devices and ICs, 2014, pp. 245-248.
[22] V. Unni, and E. M. S Narayanan, Proc. International Seminar on Power Semiconductors, 2016.
[23] V. Unni, and E. M. S. Narayanan, Proc. Wide Bandgap Semiconductor and Components Workshop, 2016.
[24] B. J. Baliga, Fundamentals of Power Semiconductor Devices, (Springer, New York, 2008), chap. 1.
[25] Tanaka K., Morita T., Umeda H., Kaneko S., Kuroda M., Ikoshi A., Yamagiwa H., Okita H., Hikita M., Yanagihara M., Uemoto Y., Takahashi S., Ueno H., Ishida H., Ishida M. and Ueda T, Appl. Phys. Lett. **107**, 163502 (2015).
[26] N. Mohan, T. M. Undeland, W. P. Robbins, Power Electronics: Converters, Applications, and Design, (John Wiley & Sons, USA, 2003), chap. 7.
[27] B. Hughes, R. Chu, J. Lazar, K. Boutros, Proc. Int. Electron Device Meeting, 2015, pp. 434-437.
[28] W. Zhang, X. Huang, F. C. Lee and Q. Li, Proc. IEEE Applied Power Electronics Conference and Exposition, 2014, pp. 1484-1489.
[29] Z. Liu, X. Huang, W. Zhang, F. C. Lee, and Q. Li, Proc. IEEE Applied Power Electronics Conference and Exposition, 2014, pp. 168-173.
[30] W. Chen, K. Y. Wong, and K. J. Chen, IEEE Electron Device Lett., **30**, 430 (2009).
[31] Y. Uemoto, T. Morita, A. Ikoshi, H. Umeda, H. Matsuo, J. Shimizu, M. Hikita, M. Yanagihara, T. Ueda, T. Tanaka, and D. Ueda, Proc. IEEE International Electron Devices Meeting, 2009, pp. 1-4.
[32] K. Y. Wong, W. Chen, X. Liu, C. Zhou, and K. J. Chen, Phys. Status Solidi B, **247**, 1732 (2010).
[33] S. Ujita, Y. Kinoshita, H. Umeda, T. Morita, S. Tamura, M. Ishida, and T. Ueda, Proc. Int. Symp. Power Semiconductor Devices and ICs, 2014, pp. 51-54.
[34] A. Nakajima, S. Nishizawa, H. Ohashi, H. Yonezawa, K. Tsutsui, K. Kakushima, H. Wakabayashi, and H. Iwai, Proc. Int. Symp. Power Semiconductor Devices and ICs, 2014, pp. 241-244.
[35] H. Hahn, B. Reuters, S. Kotzea, G. Lükens, S. Geipel, H. Kalisch, and A. Vescan, Proc. Device Research Conference, Santa Barbara, 2014, pp. 259-260.